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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,243	07/08/2003	Tohru Ueda	829-611	6228

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EXAMINER	
KIM, RICHARD H	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/614,243	UEDA ET AL.	
	Examiner	Art Unit	
	Richard H. Kim	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on March 14, 2005.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-5, 7-9, 19-21, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Fukata et al. (US 6,518,081 B2).

Referring to claims 1 and 19, Fukata et al. discloses an active matrix substrate for use in a liquid crystal display unit (col. 1, 11-17). Since Fukata et al. teaches that the board is used in liquid crystal display units, the counter substrate and a liquid crystal layer interposed between the active matrix substrate and the counter substrate are inherent. Fukata et al. also teaches that the active matrix substrate includes a plate (1), a thin film transistor (5) and a light shield layer for covering at least a portion of a side surface of the thin film transistor (7), wherein the side light shielding layer is substantially vertically oriented (7).

Referring to claims 2 and 20, Fukata et al. discloses a device wherein the active matrix substrate further includes a semiconductor layer, and the thin film transistor includes a part of the semiconductor layer (5).

Referring to claim 3, Fukata et al. discloses a device wherein the thin film transistor includes a gate electrode (col. 2, line 49), a source electrode (13), and a drain electrode (14), and the active matrix substrate further includes a pixel electrode (col. 2, line 20), a gate line acting as the gate electrode of the thin film transistor (8), and a signal line connected to the source electrode of the thin film transistor (10).

Referring to claims 4 and 21, Fukata et al. discloses a device and method wherein the active matrix substrate includes an insulating layer provided on the plate having a stepped portion having a side wall substantially perpendicular to the plate ((4); the semiconductor layer is provided on the stepped portion of the insulating layer (5); and the side light shielding layer is provided along the side wall of the stepped portion of the insulating layer (7).

Referring to claim 5, Fukata et al. discloses a device further including a lower light shielding layer provided below the thin film transistor (3).

Referring to claim 7, Fukata et al. discloses a device including an upper light shield layer provided on the thin film transistor (10).

Referring to claim 8, Fukata et al. discloses a device wherein the light shielding layer is provided so as to cover a side surface of the gate line (Fig. 6(b), ref. 8).

Referring to claim 9, Fukata et al. discloses a device wherein the light shielding layer is provided so as to cover a side surface of the data line (Fig. 6(a), ref. 10).

Referring to claims 25 and 26, Fukata et al. discloses a device comprising an active matrix substrate for use in a liquid crystal display unit (col. 1, 11-17). Since Fukata et al. teaches that the board is used in liquid crystal display units, the counter substrate and a liquid crystal layer interposed between the active matrix substrate and the counter substrate are inherent. Fukata et al. also teaches that the active matrix substrate includes a plate (1), a thin film transistor (5) and a light shield layer for covering at least a portion of a side surface of the thin film transistor (7), wherein an area of the transistor the side light shielding is provided along and directly contacts sidewalls of first, second and third insulating film which are disposed in different steps (4, 6, 9), wherein the side light shielding layer is substantially vertically oriented (7).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukata et al. in view of Hashimoto (US 6,587,165).

Fukata et al. discloses the device previously recited, and further discloses that the thin film transistor has an LDD structure (col. 5, line 8), but fails to disclose that that the active matrix substrate further includes an additional capacitance electrode, wherein the additional capacitance electrode is provided below the light shielding layer or between the light shielding

layer and the thin film transistor, wherein the additional capacitance electrode is connected to the thin film transistor, wherein the side light shielding layer is in contact with the additional capacitance electrode.

Hashimoto discloses an auxiliary capacitance (13) and its connection to lower light shield layer (5), wherein the additional capacitance is provided between the light shielding layer and the thin film transistor (13), wherein the additional capacitance electrode is connected to the thin film transistor (13), and the light shielding layer is connected with the additional capacitance (12a, 12b).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ an additional capacitance electrode, wherein the additional capacitance electrode is provided below the light shielding layer or between the light shielding layer and the thin film transistor, wherein the additional capacitance electrode is connected to the thin film transistor, wherein the side light shielding layer is in contact with the additional capacitance electrode since one would be motivated to prevent light leakage. Furthermore, Applicant has claimed multiple embodiments as to the location of the capacitor. Therefore, the precise of location of the capacitor, whether it is above or below the light shielding film, is not a critical limitation.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukata et al. in view of Sato (US 5,506,165).

Fukata et al. disclose the device previously recited, but does not disclose that the side light shielding layer is in contact with the lower light shielding layer.

Sato discloses a device wherein the light shield layer (10) contact the lower light shield layer (Fig. 3d, col. 6, lines 14-16).

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the side light shield layer to contact the lower light shield layer since one would be motivated to prevent breakdown of the drain of an MOS transistor (col. 1, lines 58-60).

6. Claims 16-18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukata et al.

Referring to claim 16-18, Fukata et al. discloses the device previously recited, and further discloses that the side light shielding layer has a two component structure (7) and is made of metal (col. 8, line 21), but fails to disclose that the light shield layer are made of polycrystalline silicon or metal silicide.

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the light shield layer to be made of polycrystalline silicon, metal or metal silicide since Fukata et al. discloses that the light shielding layer is made of the same material as the gate line (col. 4, lines 49-50). Gate lines, as is commonly known in the art is made of metal, due to its high conductive properties. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made for the light shield layer to be made of polycrystalline silicon, metal or metal silicide since one would be motivated to employ a material having high reflectivity. Moreover, Applicant has disclosed multiple materials that can be used for the light shielding material. Therefore, the specific type of material used for the light

shielding layer, whether it be polycrystalline silicon, metal or metal silicide is not a critical limitation.

Referring to claim 22, Fukata et al. discloses the method previously recited, and further discloses the step of forming the light shielding layer includes the step of forming a layer of a material of the side light shielding layer so as to cover the stepped portion of the first insulating layer (7). However, the reference does not disclose partially removing the layer by dry etching.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to partially remove the layer by dry etching since Fukata et al. discloses that light shielding layer is etched (col. 8, lines 10-11). Therefore, removing part of the layer by dry etching would been obvious since one would be motivated to achieve precise dimensions of the light shielding layer.

7. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukata et al. in view of Kim (US 6,587,165).

Fukata et al. disclose the method previously recited, but fails to disclose a second insulating layer or the flattening of the second insulating layer by chemical mechanical polishing.

Kim discloses a method of manufacturing semiconductor device capable of improving planarization, teaches the use of a second insulating layer (27) and a planarization process by chemical mechanical polishing (CMP) technique (col. 3, lines 30-35).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the chemical mechanical polishing technique to planarize the second insulating layer as taught by Kim to the device of Fukata to achieve a high degree of

integration of semiconductor devices and a low-temperature planarization process such as CMP (col. 1, lines 16-33).

Response to Arguments

8. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard H. Kim whose telephone number is (571)272-2294. The examiner can normally be reached on 9:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard H Kim
Examiner
Art Unit 2871

RHK

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER